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ARTICLE

THE SEMICONDUCTOR CHIP PROTECtION ACT: PAST, PRESENT, AND FUTURE

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I. INTRODUCTION

Throughout its legislative history, the Semiconductor Chip Protection Act of 1984 ("SCPA" or "Chip Act") generated considerable interest among businessmen and lawyers. Substantial litigation was anticipated following its enactment in November 1984; however, eight years later, only one published case, *Brooktree v. Advanced Micro Devices, Inc.*, has been decided and the initial excitement has given way to largely academic interest.[1]

This result should astonish lawmakers who in 1979 heard testimony that piracy of chip designs was a widespread problem. Where have all the pirates gone? Have they been driven from the industry by the certainty that design protection exists? Perhaps some U.S. industry leaders, apprehensive of an untried and ambiguous law, have decided to pursue other defenses in their ongoing battle with domestic and foreign competition. While these factors would arguably reduce incidents of piracy or the filing of infringement claims, they cannot explain, without more, the dearth of litigation under the Chip Act.

This Article scrutinizes the SCPA and its legislative history. An examination of the law's interaction with semiconductor technology reveals good reason for the Chip Act's lack of use. The Article also looks to the future and speculates on where the SCPA is going. The discussion begins with an overview of the elements of an infringement claim under the Act and the reverse engineering defense. Part III considers the forces that drove the domestic industry to seek protection for its designs, and reviews early chip protection bills and the SCPA legislative hearings. Part IV sets forth background material for evaluating the SCPA by focusing on semiconductor design and fabrication technology and the mechanical reverse engineering process. Part V examines semiconductor technology against the backdrop of the SCPA and its legislative history. In so doing, it exposes the suspect foundation upon which the SCPA rests-the piracy model and its supporting examples. The Article concludes that:

(1) One of the central examples of chip piracy presented at the 1979 congressional hearing actually represented bona fide non-infringing reverse engineering rather than piracy.

(2) Semiconductor designs which existed at the time the SCPA was initially proposed, and upon which the SCPA qualitative piracy model is apparently based, were susceptible to slavish copying.[2]

(3) Advances in semiconductor technology since 1979 now make slavish copying largely impossible. At one time, copyists who appropriated layout designs via mechanical reverse engineering[3] could reproduce a functioning equivalent with minimal forward engineering effort.[4] However, with contemporary semiconductor processes, the copyist must expend substantial resources analyzing an appropriated mask work in order to successfully reproduce it.

(4) Early apprehension over the efficacy of the SCPA may now be dispelled in view of the successful application of the Act in *Brooktree* and the award of $26 million in damages.

(5) Even though the slavish copying problem has been halted, the inherent burdens in forward engineering a contemporary design mean that one who engages in "barren copying" and appropriates a competitor's layout but only invests enough forward engineering to produce a functioning chip, may receive the protection of the Chip Act's reverse engineering defense. This Article questions the fairness of barren copying, but notes that proper application of the Act's infringement test could still provide a remedy in certain cases.

(6) With advances in semiconductor hardware and software design tools, the SCPA will likely find application combating a newly emerging form of slavish copying. Ironically, it appears that technological advances, responsible for ending the slavish copying problem, may once again provide "unskilled" copyists with the capability to slavishly copy a semiconductor layout design.

(7) Finally, several issues must be resolved before the SCPA can find broader application. The most significant of these is administrabilty of the Act's "substantial identicality" infringement test. The author contends that "substantial identicality" was not intended as a shorthand for "no infringement" but is an acknowledgment by Congress of the striking visual similarities inherent between semiconductor designs having the same form, fit, and function.

II. OVERVIEW OF THE SEMICONDUCTOR CHIP PROTECTION ACT

A. Elements of an SCPA claim

The SCPA provides intellectual property protection for the costly and time-consuming process of designing the circuitry embodied in semiconductor integrated circuits ("chips"). Under the Act, protection is extended to "a mask work fixed in a semiconductor chip product."[5] Mask works[6] are used in semiconductor fabrication much like stencils to create different layers of structure which collectively comprise a chip's electronic circuitry.[7]

The SCPA extends protection only to original mask works. Designs that are commonplace in the semiconductor industry, or variations of such designs that-taken as a whole-are not original are ineligible for protection.[8]

Under the Act, a mask work owner has the exclusive rights-or may grant another the rights-to reproduce the mask work and import or distribute a semiconductor chip which embodies the mask work.[9] Protection, lasting for ten years, attaches when the mask work is either registered with the Copyright Office or commercially exploited, whichever occurs first.[10]

B. The Reverse Engineering Defense

The SCPA reverse engineering defense, codified at 17 U.S.C. § 906,[11] is the principal limitation on a mask work owner's exclusive right to prevent others from reproducing, importing, or distributing the original mask work. Under § 906(a)(1), a competitor may reproduce a mask work for the purpose of analyzing it.[12] This section is analogous to copyright's fair use doctrine[13] in that it allows a competitor to reproduce a protected work for research or educational purposes. However, the SCPA enables competitors to go beyond merely studying protected works. Section 906(a)(2) permits competitors to incorporate the results of their reverse engineering analysis into subsequent *original* mask works.[14]

Section 906(a)(2) reverse engineering "carves out" a substantial limitation to a mask work owner's exclusive rights. So long as a competitor incorporates § 906(a)(1) reverse engineering analysis into an "*original*" mask work, it is free to reproduce elements of a protected mask work in a new design without fear of infringing under the Act.

1. Defining a § 906(a)(2) "original" mask work

Since a mask owner's rights under the Chip Act are limited by a competitor's right to reverse engineer, exactly what constitutes "reverse engineering" is critical to an SCPA claim. Although a lawful reverse engineering defense does *not* immunize a defendant from liability, it clearly can present a formidable obstacle to successfully proving infringement under the Act.

Giving content to "reverse engineering protection" depends on the interpretation of "original mask work" in § 906(a)(2). Unfortunately, the statute supplies no guidance in this area. However, the Act's legislative history contains two sources of information that clarify its meaning: the House Report accompanying H.R. 5525,[15] the bill from which the SCPA was largely derived, and the Senate[16] and House[17] Explanatory Memoranda.

2. The House Judiciary Committee Report

One interpretation of "original mask work" is the literal one conveyed by a plain reading of the text. However, must a mask work be "original" in this dictionary sense?[18] The answer is clearly "no." One commentator has argued against construing the House Report's originality requirement as meaning that "no part of the defendant's work may be copied from that of the plaintiff's, but only that defendant's work must also contain matter which is original to the defendant."[19] This suggests what "original" is not, but stops short of providing an analytic basis for determining what an original mask work is.

However, such an analytical framework exists in the House Report. The Committee framed its discussion of reverse engineering around two "*polar*" types of reverse engineering: "photographic reproduction of the layout of the original chip and direct incorporation thereof into a second chip"; and "making improvements on, or at least alternatives to, an existing chip and incorporating substantial but not identical parts of its design into the second chip."[20] The Committee stated its intent "to permit and encourage the second type of conduct,"[21] thereby implying that it would prohibit the first type of behavior: reproducing an original mask work and directly incorporating it into a second chip.

The notion that the SCPA allows the second type of conduct, the substantial appropriation of and improvement upon an original mask work, receives further support from the Report:

> It is the intent of the Committee to permit, under the reverse engineering limitation, the "unauthorized" creation of a second mask work whose layout, in substantial part, is similar to the layout of the protected mask work-if the second mask work was the product of substantial study and analysis, and not the mere result of plagiarism accomplished without such study or analysis.[22]

This suggests a two-step inquiry. First, if it is determined that a competitor has substantially studied and analyzed a protected mask work to produce its own chip, i.e. valid reverse engineering, that chip does not infringe even if it is substantially similar to the mask owner's. However, if the competitor's design incorporates identical parts of the protected design, infringement may yet be found.

3. The Congressional Explanatory Memoranda and the new Substantially Identical Standard

House and Senate Explanatory Memoranda, developed after the House Judiciary Report, corroborate this interpretation. They also provide additional guidance for what constitutes infringement:

> The end product of the reverse engineering process is not an infringement, and itself qualifies for protection under the Act, if it is an original mask work, as contrasted with a substantial copy. If the resulting semiconductor chip product is not substantially identical to the original, and its design involved significant toil and investment so that it is not a mere plagiarism, it does not infringe the original chip, even if the layout of the second chip is, in substantial part, similar. As noted in the Senate report, the courts are not likely, as a practical matter, to find it unduly difficult to draw the line between reverse engineering and infringement, because the additional work required to come within the privilege established by § 906(a) will ordinarily leave a "paper trail."
>
> Of course, apart from the foregoing, the amendment, like both bills, incorporates the familiar copyright principle of substantial similarity. Although, as a practical matter, copying of an insubstantial portion of a chip and independent design of the remainder is not likely, copying of a material portion nevertheless constitutes infringement. This concept is particularly important in the semiconductor chip industry, where it may be economical, for example, to copy 75% of a mask work from one chip and combine that with 25% of another mask work, if the copied parts are transferable modules, such as units from a cell library.
>
> As the Senate report notes, no hard and fast percentages govern what constitutes a "substantial" copying because substantial similarity may exist where an important part of a mask work is copied even though the percentage copied may be relatively small. Nonetheless, mask work owners are protected not only from wholesale copying but also against piecemeal copying of substantial or material portions of one or more mask works.[23]

This excerpt from the Explanatory Memoranda introduces the infringement test of "substantial identicality." As described, this test applies only when there has been a case of reverse engineering, i.e., where the defendant produces a *paper trail* that its design involved *substantial toil* and *investment*. In that instance, the copyist's chip, even if substantially similar to a protected mask work from which it derives, does not infringe so long as it is not *"substantially identical*."

The memorandum further states that "apart from the foregoing, the amendment . . . incorporates the familiar copyright principle of substantial similarity." In other words, when a copyist cannot prove it reverse engineered, its chip infringes the mask owner's if it is substantially similar. Reverse engineering is an affirmative defense.[24] The defendant bears the burden of persuasion and of presenting evidence that its design required substantial toil and investment.[25]

III. DEVELOPMENTS LEADING TO PASSAGE OF THE SCPA

A. Industry Forces and the Perceived Need for Protection Against Unfair Copying

1. Semiconductor Industry Product Cycles

Semiconductor industry products share a common life and pricing cycle. First, a pioneer introduces an innovative product which creates a new market. Early chips are handsomely priced so that the manufacturer can recoup its investment as rapidly as possible. Later, as the manufacturer becomes more efficient it cuts prices to expand its market and discourage competition. Nonetheless, second-source products-chips electrically and mechanically compatible with the pioneering product-eventually appear on the market. The arrival of competition precipitates further rounds of price cuts.[26]

2. The Benefits of Copying

The integrated circuit industry arose largely without the benefit of patent[27] or copyright[28] protection for its designs. Pioneering companies had long believed that many second-source products were the result of unfair copying. However, the need for chip protection took on a sense of urgency in the face of two developments. First, the cost of marketing and designing a state-of-the-art chip design began to skyrocket. By 1983, independent development of a cutting-edge design could cost anywhere from $40 million[29] to $50 million,[30] but could be copied for $50,000 to $100,000 in three to six months.[31] As a result, pioneering companies facing competition from copycat imitators were forced to cut prices before they could recover their investment and gain learning curve efficiencies. Second, U.S. firms began to perceive that time-saving and cost-saving advantages of unfair copying were the primary

explanation for sales and market share losses to foreign competition.[32] As one commentator stated in 1985:

> The domestic industry had pioneered the standard random access memory (RAM) chip, which became a staple product of the industry by serving as the operating basis for a variety of consumer products from personal computers to video cassette recorders. By copying this chip product, the Japanese competitors were able to enter the United States market without incurring the design and marketing costs. Given the superior quality control of the Japanese firms, they were able to offer a better product at a lower price. An increased market share and a higher ranking in the industry statistics followed.[33]

3. Early Attempts at Legal Protection

Prior to 1977, the Copyright Office registered integrated circuit designs submitted in the form of layout drawings or masks, but advised copyright applicants that, in its opinion, such registrations did not cover the final chip product.[34] In 1977, Intel Corporation attempted to register several new integrated circuit designs by submitting the designs to the Copyright Office in chip form. The Office refused registration on the ground that the chip's artistic features embodied in the chip were not conceptually separated from their utilitarian aspects.[35] Thus, the designs failed to qualify as copyrightable subject matter in that they did not meet the definition of pictorial, graphic or sculptural works under 17 U.S.C. § 101.[36] Intel filed a mandamus action to compel registration[37] but dismissed the lawsuit without prejudice when H.R. 14,293, a bill extending the Copyright Act to semiconductor designs, was introduced.[38] The bill proposed to protect chip designs by adding photographic mask works to the list of copyrightable subject matter set forth in 17 U.S. C. § 102.[39] H.R. 14,293 contained no reverse engineering provision, but impliedly incorporated the Copyright Act's fair use provision. No action was taken on H.R. 14,293 before the 95th Congress adjourned.

B. An Overview of the SCPA Legislative History

1. The 1979 San Jose Hearing

a. Dissension

H.R. 1007,[40] identical to H.R. 14,293, was introduced during the next congress. Members of a House Judiciary Subcommittee held a hearing on April 16, 1979, to solicit testimony from industry representatives.[41] Subcommittee members were surprised to find sharply divided industry opinion on whether copyright protection for chip designs was beneficial. Opponents of the bill feared that the legislation would outlaw the industry practice of reverse engineering;[42] they also expressed doubt whether protection would deter foreign copying of U.S. companies' chips and sales of them in other countries.[43] Several industry representatives commented on the short advance notice they had been given to prepare for the hearing.[44] One industry supporter of H.R. 1007 responded to a lawmaker's inquiry into the industry's differing views on chip protection by openly accusing a company opposed to the bill of having pirated its designs in the past.[45] Stymied by the industry infighting, legislative chip protection efforts came to a halt. No meaningful congressional action was taken for the next three and one-half years.[46]

b. The 1979 San Jose Hearing Concept of Piracy and Reverse Engineering[47]

At the San Jose Hearing, protectionist sentiment was voiced concerning the moral bankruptcy[48] of those who engaged in wholesale copying of their competitor's designs. Such pirates, it was explained, would make blowup photographs of a chip's top layer and copy the photo line-by-line.[49] "Line-by-line" copying, however, was distinguished from the acceptable practice of "reverse engineering."[50] Unfortunately, only one H.R. 1007 witness defined reverse engineering for the subcommittee.[51] That definition, consistent with copyright's fair use provision, was highly restrictive; it merely allowed a competitor to study and learn from another's design.[52]

2. The 1983 House and Senate Hearings

a. Harmony

In 1983, as in 1979, Intel Corporation led the renewed fight for design protection. By rallying the 57-member Semiconductor Industry Association ("SIA"),[53] S. 1201[54] and H.R. 1028,[55] bills similar to H.R. 1007, were introduced. Both bills sought to protect chip designs by creating a new copyrightable subject matter category for mask works. The House bill contained several provisions drafted exclusively to cover mask works.[56] However, an explicit reverse engineering right was not among them. H.R. 1028 implicitly relied on the Copyright Act's fair use provision to confer such a right. By contrast, the Senate bill explicitly conferred a "right of reverse

engineering,"[57] but it limited reverse-engineering to analysis and evaluation of protected mask works.

b. The 1983 Hearings' Concept of Piracy and Reverse Engineering

Although SIA spokesmen at the House[58] and Senate[59] hearings testified to the ruinous economic effects of chip piracy, their statements failed to elaborate on the slavish copying piracy model presented in 1979. They did, however, corroborate the need to preserve the industry practice of reverse engineering. Several qualitative reverse engineering models were also presented. One witness testified that competitors should be allowed to reverse engineer chips to extract their circuit schematics, but then be required to forward engineer beyond that point.[60] Another witness stated that valid reverse engineering covered forward engineering design and manufacturing enhancements.[61]

Quantitative cost[62] and record-keeping[63] criteria were suggested as means of delimiting and proving reverse engineering. However, little testimony was given in the way of *technical criteria* for distinguishing forward engineering design and manufacturing improvements. Unfortunately, these qualitative and quantitative reverse engineering models, given by an unopposed and unified SIA, were only superficially probed by the legislators.

c. The *Sui Generis* Issue

Legislative hearings on chip protection concentrated on whether the Copyright Act should be used to protect designs embodied in semiconductor chips. Publishing,[64] data processing,[65] computer manufacturing,[66] and Copyright Office representatives[67] all expressed doubts as to the wisdom of extending the Copyright Act to this end. One witness contended that reverse engineering did not fit within the copyright concept of "fair use" without a wholesale distortion of that doctrine's role and parameters.[68]

It was the testimony of Emory University Law Professor L. Ray Patterson, however, that Congress found persuasive.[69] Conceding from a constitutional standpoint that copyright is an author's right, Patterson observed that the Supreme Court had ruled that copyright's primary purpose is to benefit the public.[70] However, Patterson noted that copyright had historically inured to the benefit of publishers. This conceptual weakness between form and function, he argued, would be further eroded if explicitly utilitarian articles, such as mask works, were to become copyrightable subject matter.[71]

In April 1984, the House substituted H.R. 5525[72] for H.R. 1028. The new bill added a separate, independent, and *sui generis* chapter to 17 U.S.C. exclusively to protect mask work designs. H.R. 5525 included a reverse engineering provision, an optional notice requirement, and mandatory registration within two years of first commercialization. The Senate later yielded on the *sui generis* issue and made extensive incorporations of H.R. 5525 into its bill.[73] Both Houses of Congress added Explanatory Memoranda and passed the legislation unanimously. The President signed the SCPA into law on November 9, 1984.[74]

IV. AN OVERVIEW OF SEMICONDUCTOR DESIGN AND PROCESS TECHNOLOGY

This section provides background on semiconductor design and process engineering that is useful in appreciating the legal arguments drawn in this article.[75]

A. Forward Engineering a Semiconductor Design

1. Systems Level Design

Integrated circuit design has traditionally been a lengthy labor-intensive process which is inherently subject to error.[76] A new chip design commences with a market study of the functions that potential customers will purchase. The functions are then analyzed by a system designer to determine if they can be satisfied by an integrated circuit. When a design is large enough, the designer has an additional degree of freedom of partitioning the functions into a family of chips to lower the total cost of the system.[77]

2. Functional Block Design

The specifications of chips, such as a complex microprocessors, are defined through the use of block diagrams.[78] These diagrams depict high level modules or functional blocks such as arithmetic logic units (ALUs)[79] and shift registers.[80]

One of the most important features of the block diagram is its use as a floor plan for the chip. The floor plan expresses the spatial

relationship of the high level functional modules to one another. The area on the floor plan allocated to each functional block is determined largely by estimating the number, type, and size of transistors in the block along with their interconnections.[81]

Some of the major factors that influence a floor plan are the data path,[82] modules that must share a common bus,[83] the number of signal interconnections between functional modules,[84] and the presence of large memory block[85] of RAM[86] or ROM.[87] The final product must also mechanically[88] and electrically interface[89] with the remainder of the system.

3. Logic design

After the block diagrams are completed, the logic, circuit, and layout representation of each functional module is successively engineered. The first step is translation of the high level modules into corresponding collections of logic gates, each of which performs a simple logical operation.[90] Representations of these gates and their connections are graphically entered into a computer database to create a logic diagram or logic schematic. The logic diagram is then translated into a "netlist"[91] which contains the complete description and interconnection of all the logic gates in the schematic.[92]

a. Logic Simulation/Timing Verification

Computer simulations are then performed on the netlist to verify that the logic diagram is correct and that the circuits are "timed" properly. Timing verification is performed to detect portions of the design that could produce logic "race" conditions.[93] With increasing complexity of designs, timing verification has become much more difficult.[94]

b. Circuit Testing/Test Pattern Generation

A chip must be tested before being sold.[95] Test programs must be generated and evaluated to ensure adequate verification of the chip design as well as detection of chips with manufacturing defects.[96] The effort required to create these programs depends on the complexity of the chip and the ease of visibility of the chip's inner workings from its external connections.[97] To provide increased visibility, designers now routinely add dedicated on-chip self-testing circuitry to facilitate fault grading and testing of the final product.

For Very Large Scale Integration (VLSI),[98] correct circuit design must be verified by using complex circuit simulation software.[99] In a process known as fault grading, testing programs can evaluate the coverage of simulation test patterns by determining the percentage of faults which would be uncovered by a given set of patterns.[100] Fault simulation engines employing multiple high-speed microprocessors are available to reduce the long testing process.[101] Designers can also evaluate the circuit structure, classify likely faults, and select additional complementary test patterns. However, even with advances in diagnostic tools, circuit testing poses difficult problems, especially as chip complexity continues to escalate.

4. Circuit Design

Upon completion of the logic design, a circuit schematic designer translates each logic gate into discrete circuit components, such as transistors and interconnect.[102] A fabrication process, however, must be selected before the circuit schematic can be commenced. The fabrication process determines the layout design rules which circuits are available to the circuit schematic designer and . These fabrication design rules constrain the circuit schematics produced and their implementation by the layout designer. [103]

5. Layout Design

The layout designer translates the circuit schematic elements into corresponding types of material on the chip, where each type of material is represented by a two-dimensional set of polygons.[104] The designer graphically inputs and edits ("digitizes") the chip layout on a computer database, similar to that used for schematic entry.[105] The polygons collectively describe the mask data which is used to pattern materials during the chip fabrication process.[106]

The layout design engineer must also work within the design rules of the chip fabrication process.[107] These rules dictate, among other things, the minimum acceptable feature sizes and minimum intralayer and interlayer distances between features.[108] Since there are upwards of 100 layout design rules for a Metal Oxide Semiconductor (MOS) process, layout design is a complex and intricate task requiring considerable expertise.[109]

Upon completion of initial layout, the graphical layout is printed at high magnification to permit manual checking of timing, power,

and additional design rules.[110] After any necessary revisions, the corrected layout data is transferred to a magnetic pattern generation (PG) tape. A mask making pattern generator then produces a magnified reticle from the PG tape data.[111] After more checking, the reticle is mounted in a photorepeat camera which optically reduces the reticle and exposes it on a photosensitive mask plate.[112] After each exposure, the mask plate is translated a discrete distance, aligned by a laser interferometer, and exposed again until the mask plate is filled with rows of identical reticle imprints.[113]

The mask work for each chip layer represents the culmination of the function block, logic, circuit, and layout design efforts. The masks are used as stencils during the manufacturing process to either deposit or remove layers of metal, semiconductor, or insulating material on to or from a silicon substrate.

B. Semiconductor Fabrication

Integrated circuit technology is physically possible because the electrical properties of silicon vary widely in the presence of negatively charged[114] or positively charged[115] materials, commonly called "dopants." Positively doped silicon conducts holes; negatively doped silicon conducts electrons.[116] Different circuit elements are created on a silicon substrate by varying the type and concentration of dopant in neighboring regions of a chip.[117] Because of the minute dimensions involved and high purities required, fabrication of semiconductor chips is a lengthy process that requires meticulous quality control.[118]

C. The Mechanical Reverse Engineering Process

To successfully enter a integrated circuit market segment with a new product, the new entry must usually be compatible with established products.[119] However, the information needed to achieve compatibility is often not publicly available.[120] Thus, aspiring competitors must gather this information another way. However, they must do so without infringing mask work rights under the SCPA. In defining acceptable reverse engineering under 17 U.S.C. § 906, lawmakers attempted to balance the need for protecting investments in mask designs with procompetition sentiment. However, reverse engineering is not a unitary concept. It consists of two clear steps. In the first step, an engineer works *mechanically* backward to understand the chip's design. In the second step, this understanding is applied to *forward engineer* a new product.

Mechanical reverse engineering generally begins with a known product and works backward through deduction and inference to reconstruct the product's design and manufacturing content.[121] In the semiconductor industry, this method of working backward can involve looking at a chip under a microscope[122] and may involve etching away and successively exposing a chips constituent layers to determine the full layout of the design.[123]

However, the method used to work backward is not important. What does matter is the *depth* to which a competitor mechanically reverse engineers. By studying the mask work layers, a competitor may reverse engineer the chip's polygons or layout geometries. From the layout it may ascertain the electronic circuits represented by the layout polygons and the sequence in which the circuits are connected. It may thus recreate the chip's circuit schematic. From that schematic it may work backwards even further and recreate the chip's logic drawings. Ironically, the deeper the reverse engineering, the greater the forward engineering burdens. Every prior stage that a copyist mechanically reverse engineers (i.e., from layout to circuit schematic to logic to function block stages) represents an additional step to traverse in the forward engineering process. However, the greater the depth of reverse engineering, the greater the potential to improve, adapt, or augment the design. Conversely, shallow mechanical reverse engineering permits only copycat recreation of a competitor's chip.

V. WEAKNESS IN THE SCPA FOUNDATION: THE SCPA PIRACY MODEL AND PIRACY EXAMPLES

A. Semiconductor Technology and the H.R. 1007 Piracy Examples

To substantiate its piracy claims at the H.R. 1007 hearing, Mostek alleged that a competitor had directly copied its 16K RAM chip. To prove this claim, it pointed to the presence in the copy of useless details[124] mistakenly left in the original which exactly overlaid the original design.[125] While these photos were not published as part of the record,[126] other illustrations of piracy were provided in the Hearing Report.[127]

One of the published examples was a 4K static RAM (SRAM) produced by Intel in mid-1977 and allegedly copied and distributed by Toshiba in early 1979. While access to the full set of mask works is needed to properly compare the chips for similarities, an analysis of the two composite photographs yields some interesting observations. The floor plans of the two chips were obviously identical. However, the organization of the SRAM is dominated by highly repetitive, high density, functionally dictated memory arrays.

Therefore, the range of expression for fashioning the floor plan of a 4K SRAM is quite limited.

Moreover, there were apparent differences in the layouts of the two chips. By simple measurement of the two photographs, it appeared that the Toshiba chip was smaller. A reduction in size leads to an improvement in performance.[128] These factors, as testified to during congressional hearings,[129] are indicative of legitimate reverse engineering. Smaller transistor feature sizes can be accomplished by either: (1) using higher resolution photolithography equipment whereby all transistors are reduced in *all directions* by the same scaling constant *K* (also known as an "optical shrink"); or (2) selectively shrinking features by innovating in the mask work design or processing steps.[130]

Measurement of the memory arrays of the two SRAM chips shows that although the horizontal lengths are equal, the vertical length of the Toshiba chip is significantly less. This difference tends to rule out Toshiba's having simply scaled its chip through the use of an optical shrink. Furthermore, Toshiba's transistor patterns appear to be laid out in vertical columns while Intel's appear to be laid out horizontally. Moreover, the Intel SRAM was fabricated with a single metal process while the Toshiba chip appears to have been made with a more advanced double metal process.[131] Finally, there was a one-and-a-half-year time lag between the initial commercial distribution of the Intel chip and the appearance of the Toshiba chip. According to testimony, this delay was sufficient for Toshiba to have legitimately reverse engineered the design: "It would take maybe 3 years, 3 1/2 years to do the original, and 1 year, maybe 1 1/2 years for the pirate to do it. . . . To do just straightforward copying like this would take 3 to 5 months."[132]

The second published example of infringement in the H.R. 1007 hearing record concerns the Soviet Union's piracy of the Intel 2107b 4K dynamic RAM (DRAM). The two designs are the same size and the Soviet chip appears to be a slavish copy of the Intel device. It is important to note that the Intel DRAM was manufactured in 1974.[133] As will be explained, the relative simplicity of 1974 designs and fabrication processes may have allowed such early integrated circuits to be slavishly copied.[134]

B. Semiconductor Technology and the Legislative History Piracy Model

1. The Legislative History Piracy Model: The Slavish Copying of Designs

At the 1979 Congressional hearing in San Jose, California, chip piracy was simplistically described as the photographic copying of designs.[135] Pirates, it was explained, would merely make a blowup photograph of a chip, trace the photo line-by-line, and feed the design information into a computer in the same manner[136] in which a layout design engineer's mask work drawings are digitized.

When design protection was revisited at Senate hearings in May 1983, the same simplistic piracy model was presented:

> Again, you would measure the first layer on your computer; you etch it away, and now you have the second layer exposed. You measure that very carefully and etch it away. You continue to do that until . . . you have the set of complete patterns.[137] . . . The problem is, once you take the pattern off, then do you just make mask and put it right back on silicon?[138]

This model implies that those who mechanically *reverse engineer* a design (i.e., by etching and measuring a competitor's design layer by layer), encounter no *forward engineering* obstacles to reconstructing the mask layers into a working chip. However, as industry opposition testimony noted in 1979, process differences[139] and the engineering intricacies[140] of semiconductor technology provides natural forward engineering barriers to slavish copying. Unfortunately, the importance of these comments went unappreciated in 1979, and the issue was not raised by Congress or by the unified SIA during the 1983 hearings.[141]

2. Recognizing the Inherent Burdens of Forward Engineering

Today, and perhaps as long ago as 1979, the increased complexity and density of integrated circuits[142] means that slavishly duplicating a mask work set, without more, is unviable. Even those with a pirate's intent-interested in appropriating as much from the originator as possible and doing minimal forward engineering-can only slavishly copy if they possess the same mask work set, design equipment and fabrication process as the originator. This is unlikely. Producing a copied mask work set on even a slightly different process would likely reveal fatal incompatibilities, such as violation of the design rules for intermask and intramask spacing and line widths.

At a minimum, a second-source must first adjust the originator's layout geometries to conform to the target process' design rules and then verify the result by running design-rule-checking computer simulations. Such adjustments often entail analysis and simulation of timing and power and generation of test patterns to verify the function of the revised layout.[143]

After the design is verified, a second-source still has significant forward engineering *process* burdens. It must now ride the learning curve of the new design's process to achieve product yields that permit competitive product pricing. With contemporary processes calling for sub-micron feature sizes,[144] and over 450 processing and 45 cleaning steps,[145] these learning curves can be long and bumpy.

VI. CONCLUSION

A. The Past

1. Ironic Timing of Chip Protection Legislation and Dubious SUPPORTING testimony

By approaching Congress in 1978 for legal protection, the domestic semiconductor industry followed in the protectionist footsteps of the sound recording (1971)[146] and typeface design (1975)[147] industries. Sound recordings[148] and typeface designs[149] have long been susceptible to piracy owing to the technical ease of their reproduction. Ironically, when chip protection was first proposed, the semiconductor industry was moving in the opposite direction; smaller feature sizes meant that chips would be technically more difficult to copy into forward engineered functioning imitations.[150] Several witnesses described these forward engineering obstacles to slavish copying at the 1979 hearing.[151] However, neither congress nor pro-protection witnesses pursued or developed this testimony during the SCPA's five-and-a-half-year legislative history.

Moreover, some of the key SCPA supporting testimony was of dubious value. For example, statements characterizing "reverse engineers" as moral implied that they somehow limit their appropriation in a principled manner. But this defies common sense. With the economic and time-saving incentives of copying, and the lack of legal protection for chip designs, it seems highly probable that-except for those few companies that continually produced new state-of-the-art designs-*everyone* was copying as much and as fast as they could.

2. The Amorphous Nature of Reverse Engineering

The Semiconductor Chip Protection Act was publicly portrayed as the United States vs. Japan,[152] the Reverse Engineers vs. Pirates, and the Moral[153] vs. Immoral. Upon reflection, these characterizations seem far-fetched in that they require an agreed upon definition of reverse engineering. To compare reverse engineering with piracy presupposes that both are permanent and unambiguous concepts. Witnesses who wished to preserve the status quo of reverse engineering implied that copying limitations were easily discernible and understood throughout the semiconductor industry. However, the disparate opinions voiced during the SCPA's history demonstrate otherwise. The legislative process tells a similar story as the initial right to reproduce chips was implicitly recognized but limited by copyright's fair use provision; then it was explicitly recognized but limited to educational and analytical purposes;[154] finally it was explicitly recognized as being applicable to all chip designs and restricted only in cases of "substantial identicality."

3. Classifying The Copying Problem by Technical Skill

Although copying another company's designs has an obvious monetary reward, the "need" to copy arises not from money but from the technological superiority of one company's products over its competitors. In 1979, this technological disparity could be overcome by slavish copying, since designs of that era could be pirated. The behavior that developed can best be understood by dividing chip manufacturers according to technical ability. Three groups emerge: pioneers and two groups of second-source copyists.

Pioneers or innovators are best known for introducing revolutionary state-of-the-art products and creating new standards for the industry. The two groups of second-source copyists can also be distinguished by technical ability into skilled and unskilled copyists.

Skilled copyists are able to take what they learn from the reverse and forward engineering process, incorporate it with their existing knowledge, and advance the state of the art. Unskilled copyists either lack the ability to learn from the reverse and forward engineering process or possess insufficient design and process expertise to generate improvements. However, in the early days of minimal forward engineering efforts, the unskilled group could still slavishly copy and produce functioning designs.

The improvements contributed by the technically skilled copyists were neither done as an act of penance for taking another's design or out of an altruistic desire to advance the state of the art. Rather, they were made for economic gain. By upgrading a design, second-sources often increased the yield of their manufacturing process. Conversely, failure of the unskilled copyists to forward engineer improvements evidences both technical and ethical deficiencies.

4. The Shifting Appropriation Line

The technological disparity among these three groups was underscored during the SCPA's legislative proceedings as pioneering and second-source domestic companies fought to influence the legal appropriation standard. Industry pioneer Intel Corp. was the driving force behind the first chip protection bills. The early bills[155] proposed to extend the Copyright Act to cover chip designs and contained no explicit reverse engineering right. Legal reverse engineering would depend upon copyright's generic fair use provision and therefore would have been quite narrow.

When chip legislation was reconsidered four years later, the Senate bill contained an explicit, albeit similarly narrow, reverse engineering right. That proposal[156] would have limited a competitor who reproduced another's chip design to merely studying the design. Over the next year and a half, however, a struggle arose within the industry over how to "strik[e] the appropriate balance between the rights of the creator and the needs of the public."[157] In response, the enacted version of the SCPA shifted the appropriation line toward public consideration by allowing competitors to reproduce a protected mask work and incorporate it into an "original" mask work.

5. Congress' Excessive Technical Reliance

Congress deserves praise for having the courage to tackle semiconductor chip legislation.[158] Nonetheless, once it accepted some form of copying as the industry's competitive norm, it should have developed usable legal criteria for distinguishing fair from unfair copying. At hearings, however, legislators avoided scientific inquiry and left technological complexities to the semiconductor community. Lawmakers, instead, dwelled on resolving the philosophical question of what form of legal protection semiconductor designs should receive. As a result, Congress failed to investigate the inherent forward engineering burdens of copying a chip design. Further, the qualitative piracy and reverse engineering models discussed at SCPA hearings were never clearly developed or assented to during the legislative process. Moreover, the basis for the SCPA-the piracy examples displayed at the 1979 hearing-was never questioned. One of Congress' two published examples of piracy probably illustrates valid reverse engineering, not piracy. The other example appears to be valid since it was based on a 1974 design and, therefore, susceptible to slavish copying.

6. The LESSON OF Brooktree

a. The Parties' Contentions

The only published dispute under the SCPA arose between Brooktree Corporation and Advanced Micro Devices, Inc. (AMD).[159] Plaintiff Brooktree owned several original mask works that were registered with the Copyright Office for SCPA protection. The masks were used to fabricate integrated circuit chips that converted digital graphics information to high frequency analog information for very high resolution video screen displays. Approximately 80% of the area of the chips consisted of the core 10 transistor SRAM cell, repeated over six thousand times.[160] Brooktree alleged that AMD had misappropriated Brooktree's original mask works in producing its second source chips.[161]

b. The Decisions

Prior to trial, Brooktree sought a preliminary injunction to prevent AMD from manufacturing and distributing the disputed chips. AMD challenged the motion claiming that its chip designs were the product of reverse engineering and therefore noninfringing. In support of its reverse engineering defense, AMD produced a paper trail of evidence showing that it had invested over fifteen months time and an equal or greater amount of money than Brooktree did in developing their chips.[162] Brooktree argued that the paper trail evidence demonstrated only AMD's incompetent efforts and should, therefore, be disregarded.[163]

The court ruled that AMD's paper trail was sufficient to require plaintiff Brooktree to prove that the allegedly pirated chips were "substantially identical" to the Brooktree chips and that, in light of this heightened burden of persuasion, Brooktree had failed to make a showing of a strong likelihood of success on the merits.[164] The court further ruled that Brooktree failed to establish that it was sufficiently harmed by AMD's actions to merit a preliminary injunction[165] and that monetary damages were adequate compensation if infringement was later proven.[166]

Although the court denied Brooktree's motion, it noted that "*serious questions as to the appropriate resolution of the substantive issues in the case have been raised."*[167] While Brooktree's defeat in seeking preliminary relief may have dampened interest in the SCPA, this should change in light of the case's ultimate disposition.

At trial, Brooktree faced a lower standard of proof than it did in requesting the preliminary injunction.[168] Furthermore, it received the benefit of pre-trial discovery. After a seven week jury trial, the verdict awarded Brooktree $26 million in damages for AMD's infringement under the SCPA and several patents.[169] AMD's motions for judgment notwithstanding the verdict (JNOV) and a new trial were denied by the district court and AMD appealed. The presence of patent claims gave the Court of Appeals for the Federal Circuit pendent jurisdiction over the SCPA cause of action.[170]

On appeal, AMD asserted it was undisputed that: at least 20% of the chip was not copied; the SCPA "requires copying of the entire chip," as a matter of law, to establish substantial similarity for the purpose of finding infringement; and, therefore, the judgment of infringement was in error.[171] The court rejected this argument, citing both general copyright law and the SCPA legislative history, and held that substantial similarity could be found from less than wholesale copying, such as the appropriation of the layout of a core cell.[172]

AMD also argued that its core cell was reverse engineered; the reverse engineering was substantiated by a voluminous paper trail; and, as a matter of law, did not infringe the Brooktree mask works.[173] The court's analysis focused on the term "original" in the Act's reverse-engineering statutory defense.[174] The court rejected AMD's argument and ruled that "the paper trail is evidence of independent effort, but it is not conclusive or incontrovertible proof of originality."[175] At trial, the jury was instructed to place "great weight" on AMD's paper trail in determining originality.[176] After acknowledging that credible conflicting testimony had been presented regarding the similarity of the core cells, the pertinence of AMD's paper trail, and whether AMD's chips contained improvements, the court held that "reasonable minds could draw different conclusions" as to the originality of AMD's design.[177] This being the case, the judgment was affirmed.

c. The Legacy of *Brooktree*

The absence of a single additional SCPA case apart from *Brooktree* suggests that the intellectual property bar may have been awaiting its final adjudication before adding SCPA claims to their litigation arsenal. However, since *Brooktree* was tried to a jury, there is no possibility of scrutinizing the decisional process leading to the finding of infringement. Moreover, since the jury instructions went unchallenged on appeal, the Federal Circuit had little opportunity to develop the reverse-engineering doctrine. We know from *Brooktree*, that it is not necessary to copy an entire chip to infringe under the Act. Moreover, we know that paper trail evidence alone does not establish the reverse engineering defense.

B. The Present

The Chip Act's legislative history suggests that the "substantial toil and investment" paper trail requirement was created largely to stop slavish copying. However, as discussed above, it appears that increasing integration and its concomitant forward engineering burdens, not the SCPA,[178] are responsible for closing off this form of piracy.[179]

Thus, given the present state of technology and the "substantial toil and investment" reverse engineering standard, it is reasonable to inquire as to what vitality the SCPA retains today. The answer depends on whether the SCPA was intended to only address the specific problem of slavish copying or was also meant to prohibit a competitor from copying to the extent that semiconductor technology and its accompanying design tools allow. This latter form of copying, known as "barren copying," exists when a copyist appropriates a competitor's layout through the mechanical reverse engineering process and then performs only so much forward engineering as is necessary to produce a functioning chip. The decision in *Brooktree* suggests that barren copying of a cell layout can constitute infringement where there is no compelling paper trail or substantial improvement in the product.

Prior to *Brooktree*, there were concerns that the demands of existing technology, which frequently require that a barren copyist engage in substantial toil and investment to forward engineer a working chip, and the corresponding paper trail would likely satisfy the Explanatory Memoranda criteria for reverse engineering. However, *Brooktree* suggests that the paper trail review should not be done in a vacuum, but should focus on the competency of the defendant's forward engineering efforts.

C. The Future

1. Is a New Form of Slavish Copying on the Horizon?

Notwithstanding the SCPA's sparse application, two technological trends may once again enable slavish copying and therefore revitalize the SCPA as an intellectual property weapon. First, CMOS, which has been the design technology of choice for several years, is becoming mature. With maturity, the process and design secrets distinguishing different companies' CMOS technologies

become fewer and less profound. CMOS technology is becoming a commodity. As it does, slavish line-by-line copying becomes possible.

Second, and more importantly, semiconductor design and process secrets are being encoded into software that increasingly permits semiconductor designs to be created by computer. In earlier years, engineers designed circuits on paper and tested their work by constructing physical prototypes. Computer workstations which partly automate the layout process first appeared in the late 1970's. That breakthrough was followed by software which permits chips to be designed from predefined logic gates or entire blocks of circuitry rather than individual transistors. Today, a new technology called "logic synthesis" promises to free designers from the time-consuming task of connecting circuits. Starting from a textual description of a chip's functions, the software automatically creates a circuit design that performs these functions.[180] These software and hardware improvements can lessen a copyist's forward engineering burdens. Ultimately, neo-slavish copying may arise in which "unskilled" copyists can once again knock-off a chip design.

A final influence is also at work. For decades, chips have been built from bulk semiconductor materials and technological improvements have been achieved through the use of increasingly smaller transistors. In the not-too-distant future, it appears that the pace of miniaturization must slow as advancing chip technology encounters the physical limits of semiconductor materials. When transistor dimensions fall below 0.2 microns, conventional transistors fail as their behavior becomes dominated by "quantum tunneling" effects. Tunneling, a phenomenon of quantum physics, occurs when electrons penetrate solid matter and electrical barriers that, in bulk materials, are usually impassable.[181] If the quantum tunneling problem slows semiconductor advancements, software and hardware design and process equipment improvements that will continue to progress will reduce a copyist's forward engineering burdens and permit slavish copying.

2. Don't Forget the Infringement Test

This Article has focused on the Chip Act's interaction with semiconductor technology. However, of equal or greater concern is the application of an SCPA infringement test. Although this topic is beyond the present discussion, the controversy is largely a philosophical one. Congress provided no indication of what constitutes "substantial identicality" much as it failed to do with copyright law's "substantial similarity" test. Apparently, it preferred to let the courts develop the doctrine. However, there are two ways of viewing "substantial identicality."

Advocates of the first viewpoint assert that Congress intended an owner's rights under the SCPA to be narrow. They would argue that "substantial identicality" was intended as an imposing obstacle to infringement liability, a kind of shorthand for "no infringement." It would then follow that once a defendant proved reverse engineering by a paper trail of evidence, infringement could only be found in cases involving obvious and substantial misappropriation.

The second viewpoint, to which the author subscribes, regards "substantial identicality" as an acknowledgment by Congress and the semiconductor industry of the striking visual similarities inherent in designs that perform the same functions. This group would maintain that the SCPA is infringed when a defendant's paper trail is deemed insufficient and "substantial similarity" otherwise exists. By this view, a copyist can only defend against infringement allegations by producing a sufficiently compelling paper trail. The practical importance of the SCPA among intellectual property laws likely depends upon which of these two competing viewpoints prevails.

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1. The SCPA is codified at 17 U.S.C. §§ 901-914 (1988). The only published case under the Act arose between plaintiff Brooktree Corporation and defendant Advanced Micro Devices, Inc. (AMD). In that case, a jury awarded Brooktree $26 million as damages for AMD's infringment under the SCPA and several patents. Greg Johnson, *Jury Awards Brooktree $26 Million in Damages*, L.A. TIMES, Sept. 29, 1990, at B2. The litigation resulted in the following published decisions: Brooktree Corp. v. Advanced Micro Devices, Inc., 705 F. Supp. 491 (S.D. Cal. 1988) (denying Brooktree's motion for a preliminary injunction); Brooktree Corp. v. Advanced Micro Devices, Inc., 757 F. Supp. 1088 (S.D. Cal. 1990) (denying AMD's motion for judgment notwithstanding the verdict (JNOV) and motion for new trial), *aff'd*, 977 F.2d 1555 (Fed. Cir. 1992).

2. Slavish copying is the ability to create a functioning chip from the photographic copying of mask works without additional

engineering. *See infra* part V.B.

3. Mechanical reverse engineering is the process of starting with a known product and working backward to deduce the process which aided in its development or manufacture. *See infra* part V.B.

4. Forward engineering is the orderly process of conceiving and designing a semiconductor design. It progresses from the system level (market study) through function block , logic schematic, circuit schematic, and layout stages. *See infra* part IV.A.

5. 17 U.S.C. § 902(a)(1) (1988).

6. A mask work is defined under the Act as:

> a series of related images, however fixed or encoded-
>
> (A) having or representing the predetermined, three dimensional pattern of metallic, insulating, or semiconductor material present or removed from the layers of a semiconductor chip product; and
>
> (B) in which series the relation of the images to one another is that each image has the pattern of the surface of one form of the semiconductor chip product.

Id. § 901(a)(2).

7. *See generally infra* part IV (discussing semiconductor design and fabrication).

8. 17 U.S.C. § 902(b) (1988).

9. *Id.* § 905.

10. *Id.* § 904(a)-(b).

11. *Id.* § 906.

> 12. Notwithstanding the provisions of § 905, it is not an infringement of the exclusive rights of the owner of a mask work for-
>
> (1) a person to reproduce the mask work solely for the purpose of teaching, analyzing, or evaluating the concepts or techniques embodied in the mask work or the circuitry, logic flow, or organization of components used in the mask work . . . .

Id. § 906(a).

> 13. Notwithstanding the provisions of section 106, the fair use of a copyrighted work, including such use by reproduction in copies or phonorecords or by any other means specified by that section, for purposes such as criticism, comment, news reporting, teaching (including multiple copies for classroom use), scholarship, or research, is not an infringement of copyright. In determining whether the use made of a work in any particular case is a fair use the factors to be considered shall include-
>
> (1) the purpose and character of the use, including whether such use is of a commercial nature or is for nonprofit educational purposes;
>
> (2) the nature of the copyrighted work,
>
> (3) the amount and substantiality of the portion used in relation to the copyrighted work as a whole; and
>
> (4) the effect of the use upon the potential market for or value of the copyrighted work.

Id. § 107.

14. "[I]t is not an infringement . . . for . . . a person who performs the analysis or evaluation described in paragraph (1) to incorporate the results of such conduct in an original mask work which is made to be distributed." *Id.* § 906(a).

15. The House Report accompanying Pub. L. No. 98-781 was taken from the report that accompanied H.R. 5525. That bill was approved by the House Committee on the Judiciary on May 15, 1984, and passed by the full House on June 11, 1984. *See* HOUSE COMM. ON THE JUDICIARY, SEMICONDUCTOR CHIP PROTECTION ACT OF 1984, REPORT TO ACCOMPANY H.R. 5525, H.R. REP. NO. 781, 98th Cong., 2nd Sess. (1984), *reprinted in* 1984 U.S.C.C.A.N. 5750 [hereinafter H.R. 5525 REP.].

16. 130 CONG. REC. 28,959 (1984) (explanatory memorandum to the Mathias-Leahy Amendment to S. 1201). The House and Senate Memoranda are nearly identical.

17. 130 CONG. REC. 30,945 (1984) (explanatory memorandum of the Senate Amendment to H.R. 6163, title III, as considered by the House of Representatives) ("Kastenmeier Explanatory Memorandum").

18. *Webster's Ninth New Collegiate Dictionary* (1983) defines the adjective "original" as "1: of, relating to, or constituting an origin or beginning; 2a: not secondary, derivative, or imitative b: being the first instance or source from which a copy, reproduction, or translation is made 3: independent and creative in thought or action."

19. 3 MELVILLE B. NIMMER & DAVID NIMMER, NIMMER ON COPYRIGHT § 18.06[D], at 18-32.1 (1992).

20. H.R. 5525 REP., *supra* note 15, at 22.

21. *Id.*

22. *Id.*

23. 130 CONG. REC. 28,960 (1984).

24. H.R. 5525 REP., *supra* note 15, at 23.

25. Leo J. Raskind, *Reverse Engineering, Unfair Competition and Fair Use*, 70 MINN. L. REV. 385, 398-99 (1985).

26. This cycle has been dubbed "learning-curve" pricing. *See* Robert W. Kastenmeier & Michael J. Remington, *The Semiconductor Chip Protection Act of 1984: A Swamp or Firm Ground?*, 70 MINN. L. REV. 417, 452-53 (1985).

27. Patent law does not protect semiconductor layouts because the creativity involved ordinarily does not meet the patent requirements of being new, useful, and nonobvious. H.R. 5525 REP., *supra* note 15, at 3.

28. Mask works are utilitarian articles and, therefore, fall outside the scope of copyright protection. *Id*. at 15.

29. Nadine Cohodas, *Special Report: Technology and the Law-New Technology Puts Strain on Old Laws*, 42 CONG. Q. 135 (1984).

30. *Copyright Protection for Imprinted Design Patterns on Semiconductor Chips: Hearings on H.R. 1007 Before the Subcomm. on Courts, Civil Liberties and the Admin. of Justice of the House Judiciary Comm.*, 96th Cong., 1st Sess. 135 (1979) [hereinafter *H.R. 1007 Hearings*] (statement of Richard H. Stern). If 1983 estimates were correct, then it is likely that development costs for cutting-edge designs today reach or exceed $100 million. *See* H.R. 5525 REP., *supra* note 15, at 2.

31. *The Semiconductor Chip Protection Act of 1983: Hearings on S. 1201 Before the Subcomm. on Patents, Copyrights and Trademarks of the Senate Judiciary Comm.*, 98th Cong., 1st Sess. 66, 75-76 (1983) [hereinafter *S. 1201 Hearings*] (statement of Thomas F. Dunlap, General Counsel, Intel Corp.); *id.* at 78-79 (statement of Dr. Christopher K. Layton, Vice-President, Intersil, Inc.).

32. *See H.R. 1007 Hearings*, *supra* note 30, at 31-33 (statement of Andrew Grove, President, Intel Corp.).

One study showed that in 1978 U.S. firms occupied five of the top ten industry rankings by volume of sales. In that year, the Japanese firms ranked third, seventh, and eighth. By 1984, the Japanese firms had moved into the second, fourth, fifth, and seventh places. Raskind, *supra* note 25, at 413 (citing MICHAEL BORRUS, REVERSING ATTRITION: A STRATEGIC RESPONSE TO THE EROSION OF U.S. LEADERSHIP IN MICROELECTRONICS (1985) (Working Paper, Berkeley Roundtable on the International Economy)).

33. Raskind, *supra* note 25, at 413 (citing *S. 1201 Hearings*, *supra* note 31, at 82 (statement of F. Thomas Dunlap, Jr., General Counsel, Intel Corp.)).

For a further discussion of Japanese dominance of the RAM market, see Kathleen K. Weigner, *Is the Sun Setting on the U.S. Semiconductor Industry?*, FORBES, June 17, 1985, at 111-14.

34. "The Copyright Office historically has refused, and presently does refuse, to register claims to copyright in the design or layout of . . . and the . . . chips themselves. . . . Courts have consistently refused to extend copyright to useful articles as such." C*opyright Protection for Semiconductor Chips: Hearings on H.R. 1028 Before the Subcomm. on Courts, Civil Liberties, and the Admin. of Justice of the House Comm. on the Judiciary*, 98th Cong., 1st Sess. 88 (1983) [hereinafter *H.R. 1028 Hearings*] (statement of Dorothy Schrader, Associate Register of Copyrights for Legal Affairs).

35. H.R. 5525 REP., *supra* note 15, at 15. *See also S. 1201 Hearings*, *supra* note 31, at 29 (1983) (testimony of Dorothy Schrader, Associate Register of Copyrights for Legal Affairs).

> 36. "Pictorial, graphic and sculptural works" include two-dimensional and three-dimensional works of fine, graphic, and applied art, photographs, prints and art reproductions, maps, globes, charts, diagrams, models, and technical drawings, including architectural plans. Such works shall include works of artistic craftsmanship insofar as their form but not their mechanical or utilitarian aspects are concerned; the design of a useful article, as defined in this section, shall be considered a pictorial, graphic, or sculptural work only if, and only to the extent that, such design incorporates pictorial, graphic, or sculptural features that can be identified separately from, and are capable of existing independently of, the utilitarian aspects of the article.

17 U.S.C. § 101 (1988) ("Definitions").

37. Intel Corp. v. Ringer, No. C77-2848 (N.D. Cal. filed Oct. 10, 1978).

38. 124 CONG. REC. 36,628 (1978). The bill was introduced and the suit was discontinued on October 12, 1987.

39. The subject matter of copyright is listed under 17 U.S.C. § 102(a). That section protects "original works of authorship" which includes the following categories: "(1) literary works; (2) musical works, including any accompanying words; (3) dramatic works, including any accompanying music; (4) pantomimes and choreographic works; (5) pictorial, graphic, and sculptural works; (6) motion pictures and other audiovisual works; and (7) sound recordings."

40. *H.R. 1007 Hearings*, *supra* note 30.

41. *Id.*

42. *Id*. at 57 (statement of James M. Early, Director, Fairchild Camera & Instrument Corp.).

43. *Id*. at 51-52 (statement of John Finch, National Semiconductor Corp.).

44. *Id*. at 62 (statement of Congressman Kastenmeier).

45. Intel Corporation accused one competitor of having pirated its 8K-bit programmable reload memory chip and its 8080 microprocessor. *See id.* at 72.

46. After the H.R. 1007 hearings, chip protection efforts by the 96th Congress ceased.

The 97th Congress introduced chip protection bills in the House and Senate. *See* H.R. 7207, 97th Cong., 2d Sess., 128 CONG. REC. 26,129 (1982) (introduced by Rep. Edwards on Sept. 29, 1982); S. 3117, 97th Cong., 2d Sess., 128 CONG. REC. 32,356 (1982) (introduced by Sen. Mathias on Dec. 18, 1982). These bills were referred to each branch's Judiciary Committee and no further action was taken.

47. See *infra* part IV.B.1 for a discussion of the legislative history piracy and reverse engineering models.

48. "[V]arious members of the industry . . . have resorted to copying . . . . [O]ur company . . . has never done it . . . . [Only t]he lesser novelty segment of the industry feels it necessary to resort to it periodically." *H.R. 1007 Hearings*, *supra* note 30, at 28 (statement of Andrew Grove, President, Intel Corp.).

49. *Id*. at 26-27 (statement of L.J. Sevin, President, Mostek Corp.).

50. "We have no quarrel with [reverse engineering]. It is fair game." *Id*. at 27 (statement of L.J. Sevin, President, Mostek Corp.).

51. "We certainly reverse engineer, as do all of our competitors, which is defined as looking in great detail at competitive chips and utilizing either in future designs or improved designs, the things we learn from those chips. It is standard industry practice." *Id*. at 69 (statement of John Finch, National Semiconductor Corp.).

52. This concept of reverse engineering is also consistent with the definition advanced in Mostek Corp. v. Inmos Ltd., 203 U.S.P.Q. (BNA) 383, 386 (N.D. Tex. 1978). There, reverse engineering was described as "analyzing a competitor's product to discover its design and fabrication processes."

53. The American Electronics Association supported H.R. 1007. The SIA neither took a stand nor was represented at the 1979 hearing. *See H.R. 1007 Hearings*, *supra* note 30, at 73.

54. S. 1201, 98th Cong., 1st Sess., 129 CONG. REC. 10,974 (1983).

55. H.R. 1028, 98th Cong., 1st Sess., 129 CONG. REC. 937 (1983).

56. These new provisions included a ten-year term of protection, modified exclusive rights for mask work owners, and a compulsory licensing provision for innocent infringers. *See id.*

57. This explicit right was to be created by adding 17 U.S.C. § 119 as follows:

> (a) In the case of mask works, the exclusive rights provided by section 106 are subject to a right of reverse engineering use under the conditions specified by this section.

(b) It is not an infringement of the rights of the owner of a copyright on a mask work to reproduce the pattern on one or more masks or in a semiconductor chip product solely for the purpose of teaching, analyzing, or evaluating the concepts or techniques embodied in the mask or semiconductor chip product, or the circuit schematic, logic flow, or organization of components utilized therein.

58. *H.R. 1028 Hearings*, *supra* note 34.

59. *S. 1201 Hearings*, *supra* note 31.

> 60. A reverse engineering firm should be allowed to analyze the chip, draw a circuit schematic of the chip, and then layout a different pattern. This pattern could be used to fabricate a version of the semiconductor chip which is functionally equivalent to the original chip but has different visual patterns on it.

H.R. 1028 Hearings, *supra* note 34, at 27-28 (statement of F. Thomas Dunlap, Jr., General Counsel, Intel Corp.).

"In chip language, that would mean that a fair reverse engineering person has the right to analyze the chip, understand the chip, and

come up with the circuit schematic." *S. 1201 Hearings*, *supra* note 31, at 66 (statement of F. Thomas Dunlap, Jr., General Counsel, Intel Corp.).

"The bare fact of taking the chip and photographing the layer and etching it, and so forth, to draw out this schematic is not prohibited by the bill. . . . But if you take it off, get the schematic, and then make a different picture, that would be reverse engineering." *Id*. at 84.

61. The legitimately reverse engineered chip would be a better performing product or a smaller product and therefore less expensive to manufacture. *S. 1201 Hearings*, *supra* note 31, at 83 (statement of Dr. Christopher K. Layton, Intersil Inc.).

62. "Now, the difference between reverse engineering and direct copying is that reverse engineering is going to cost about 25 percent of the original design and it's also going to advance the state of the art." *H.R. 1028 Hearings*, *supra* note 34, at 34 (statement of F. Thomas Dunlap, Jr., General Counsel, Intel Corp.).

63. "When there is a legitimate job of reverse engineering, there is a very big paper trail, there's computer simulations, there's all kind of time records, people who spent an enormous amount of time understanding and figuring out how to make the design." *Id*. at 36.

64. *S. 1201 Hearings*, *supra* note 31, at 102-11 (statement of Jon Baumgarten, Counsel for the Association of American Publishers).

65. *Id*. at 101-02 (statement of Ronald Palenski, Association of Data Processing Organizations).

66. *Id*. at 99-101 (statement of A.G.W. Biddel, Computer and Communications Industry).

67. *Id*. at 18-25 (statement of Dorothy Schrader, Associate Register of Copyrights for Legal Affairs).

68. *Id*. at 104 (statement of Jon Baumgarten); *see also H.R. 1007 Hearings*, *supra* note 30, at 57 (statement of James M. Early, Director, Fairchild Camera & Instrument Corp.) (voicing fear that such an extension would distort traditional copyright principles, lead to interpretation problems, and erode some of the exclusive rights given to owners of conventional copyrights).

69. *See* H.R. 5525 REP., *supra* note 15, at 6.

70. Sony Corp. of Am. v. Universal City Studios, Inc., 464 U.S. 417, 429 (1984).

71. *H.R. 1028 Hearings*, *supra* note 34, at 51-54.

72. H.R. 5525 REP., *supra* note 15, at 5-7.

73. *See* 130 CONG. REC. 28,966-71 (1984) (Senate floor statements).

74. The Semiconductor Chip Protection Act was contained under title III of H.R. 6163, a five-title bill, and became Pub. L. 98-620, 98 Stat. 3335 (1984).

75. For a general discussion of semiconductor fabrication process see BILL PLETSCH, INTEGRATED CIRCUITS: MAKING THE MIRACLE CHIP (2d ed. 1985).

76. This has been changing, however, as the use of semicustom and custom computer aided engineering ("CAE") systems have been rapidly expanding in recent years.

77. Smaller chips are easier to test and design and produce a greater yield but their use must be balanced against the higher cost of handling, testing, and packaging a larger number of chips. MOS INTEGRATED CIRCUITS 331-33 (William M. Penney & Lillian Lau eds., 1972).

78. *Id*. at 333.

79. An ALU is a section of the central processing unit (CPU) that makes arithmetic and logical comparisons and performs arithmetic

functions. BRIAN SPINKS, INTRODUCTION TO INTEGRATED-CIRCUIT LAYOUT 151 (1985).

80. Shift registers displace a binary quantity one or more places to the right or left. With binary expressions it is the equivalent of multiplying or dividing the expression by two to the power of the number of spaces shifted. *Id*. at 167.

81. The number of transistors is estimated in turn from the complexity of the function to be performed by the block.

82. For example, in the central processing unit ("CPU") the floor plan is determined by the natural data path. The CPU is the brain of the computer. It fetches, decodes, and executes program instructions and maintains the status of results. *Id*. at 155.

83. Typical buses include power, ground, and signal buses. Two power busses, commonly named Vss and Vdd, provide all of the power used by an integrated circuit. *Id*. at 169-70. A signal bus consists of a collection of functionally related signals. Topologically, most of the circuitry is fabricated beneath the buses. *Id*. at 112.

84. Space must be allocated in the floor plan for interconnection routing between functional blocks. While interconnects are preferably in metal, space limitations may require use of other types of materials, such as polysilicon. THOMAS M. FREDERIKSEN, INTUITIVE IC CMOS EVOLUTION 79-80 (1984). This is called the Poly/Metal crossover, a conventional technique in the industry. *See* Eric W. Petraske, *Technical Overview*, *in* THE SEMICONDUCTOR PROTECTION ACT OF 1984, at 3 (Jon A. Baumgarten ed., 1984).

85. Memory blocks often dominate a floor plan and cannot be shrunk further. Unless speed is a critical factor, there may be little incentive to engineer decreases in the size of other modules if overall chip size will not be substantially reduced. SPINKS, *supra* note 79, at 122.

86. RAM (Random Access Memory) is:

> a static or dynamic memory device that data can be written into or read from a specific location. The specific RAM location is selected by the address applied via the address bus and control lines. Data are stored in such a manner that each bit of information can be retrieved in the same length of time. This has come to mean, by common usage, read/write memory.

Id. at 166.

87. ROM (Read Only Memory) is memory in which information is permanently stored at the time of manufacture. The information is available at any time, but cannot be modified during normal system operation. Fixed instructions are often embedded in ROM. *Id*. at 163-66.

88. "Second sourcing," whereby a semiconductor manufacturer designs a chip to be fungible with a commercially successful design, is common in the industry. The second source chip must be physically compatible with the original chip. SABURO MUROGA, VLSI SYSTEM DESIGN 41 (1982).

89. The second source chip must also operate the same equipment and perform the same functions as the original chip. For example, a timing clock, often used in dynamic logic networks, presents problems of both physical and electrical compatibility. It requires significant power and floor plan area and must have minimal unnecessary interconnect. SPINKS, *supra* note 79, at 48-49.

90. Logic gates such as AND, OR, and NOT in combination can create any Boolean mathematical operation. *Id.* at 39.

91. FREDERIKSEN, *supra* note 84, at 142.

92. *Id*. at 142.

93. Race conditions occur when a circuit's output changes too quickly to be stored by another circuit. MOS INTEGRATED CIRCUITS, *supra* note 77, at 260.

94. Logic simulation programs are available which input discrete Boolean values of 1 or 0 at chip inputs and generate the resulting values at outputs. Michael Feuer, *VLSI Design Automation: An Introduction*, PROC. IEEE, Jan. 1983, at 6.

95. *Id*.

96. FREDERIKSEN, *supra* note 84, at 142.

97. Internal access to chip circuitry can be made by microprobe (using fine metal needles under a microscope to contact metal interconnect); however, increasingly fine geometries make this a difficult process. MOS INTEGRATED CIRCUITS, *supra* note 77, at 365.

98. Very Large Scale Integration began with the appearance of chips bearing 200,000 transistors and 4-micron feature sizes in roughly 1980. SPINKS, *supra* note 79, at 2-3.

99. MOS INTEGRATED CIRCUITS, *supra* note 79, at 365-67.

100. Feuer, *supra* note 94, at 6. These programs sequentially force all internal circuit nodes at a binary 1 or 0 value. The programs then determine if the intended sequence of tests will detect these simulated faults. The percentage of the faults that are detected by the testing program is the numerical fault grade. A grade of 85% faults detected is considered acceptable. FREDERIKSEN, *supra* note 84, at 142.

101. These simulation engines can perform over 100,000 circuit emulations per second with circuits containing as many as 1,000,000 logic gates. *See* Loys Gindraux & Gary Catlin, *CAE Station's Simulators Table 1 Million Gates*, ELECTRONIC DESIGN, Nov. 10, 1983, at 127.

102. SPINKS, *supra* note 79, at 39-60.

103. *See infra* note 109 for a discussion of typical layout design rules.

104. H.R. 5525 REP., *supra* note 15, at 12.

105. DEWITT G. ONG, MODERN MOS TECHNOLOGY 323-24 (1984).

106. Feuer, *supra* note 94, at 1.

107. As changes are made, he must also work with other engineers to ensure the design is logically correct, timed properly, and does not consume too much power. MOS INTEGRATED CIRCUITS, *supra* note 77, at 400-14.

108. Layouts are governed by design rules that dictate size and dimensional relationships between layers. These rules reflect the capability of the particular process. The major design rules prescribe: (1) the minimum widths that can be routinely and reliably patterned without notching or necking (causing a break) in the line; (2) the minimum space that similar features can be routinely and reliably etched separated with no bridging, (3) minimum pitch, which equals the sum of the minimum width and the minimum space and is the true measure of the photolithography and etching capability of a process; (4) overlap required between adjacent layers, for example, in a contact diffusion where the aperture will be enlarged during etching and shrunk during the diffusion stage, so that the metal will short to the substrate layer if the diffusion does not overlap the contact by a sufficient amount; and (5) minimum distances which must separate dissimilar features because of shrinkage and enlargement during processing. Minimum space and minimum width can be played off against each other. For example, a very narrow line could be obtained by extreme over-etching but it could not be placed close to a similarly narrow line. ONG, *supra* note 106, at 319-21. An important process design parameter that influences layout design rules is mask misalignment tolerance in conjunction with the process mask work sequence. SPINKS, *supra* note 79, at 94.

109. Layout designers were described in the 1979 House hearings as "[c]reative persons and not just draftsmen . . . . Layout design is a skill that has successfully resisted . . . attempts at computerization. It requires a level of human ingenuity that will not be computerized . . . ." *H.R. 1007 Hearings*, *supra* note 30, at 26 (statement of L.J. Sevin, President, Mostek Corp.). Twelve years later, however, companies such as Synopsis Inc. of Mountain View, California, have become successful at writing design software for the layout process. *See* Don Clark, *Chip Design-A Crucial Technology*, S.F. CHRON., June 17, 1991, at B1.

110. Design rule checking is typically done by computer program, supplemented by manual checks.

111. The pattern generator writes on the reticle with a beam of light that flashes on and off at a very high rate. The reticle is then magnified between 20 and 200 times to generate transparent films called "blowbacks." The blowbacks are returned to the layout designers for a final check. ONG, *supra* note 106, at 326-28.

112. MUROGA, *supra* note 88, at 34.

113. Working copies are made from the master mask plate for actual use in the wafer processing area. *Id.*

114. For example, phosphorus, antimony, and arsenic.

115. For example, boron and gallium.

116. PLETSCH, *supra* note 75, at 38.

117. For example, an npn junction transistor consists of a layer of positive-type silicon between two layers of negative-type silicon. The inner layer is called the base; the outer layers, the emitter and the collector. Applying a positive voltage to the base and a higher positive voltage to the collector (and wiring the emitter to ground) establishes current flow. The positive holes of the base are repelled by the positive voltage of the collector into the negatively charged emitter. Electrons, attracted to the positive voltages of the base and the collector, rush out of the emitter, through the base, and into the collector. The total number of electrons is increased by the extra electrons in the doped emitter and collector. By completing the journey from emitter to collector, the current applied to the base is greatly amplified. PAUL E. GRAY & CAMPBELL L. SEARLE, ELECTRONIC PRINCIPLES: PHYSICS, MODELS, AND CIRCUITS 245-250 (1969).

118. The manufacturing process begins with the growing of a cylindrical ingot of pure silicon. After the ingot is grown a flat edge is cut along its length to serve as a reference point during the fabrication process. Next, the ingot is sliced into .025"-thick wafers which are ground smooth and polished on one side to remove scratches and contamination. An oxygen-ported oven is used to grow a thin surface oxide layer on the wafer. The oxide layer allows materials to be selectively diffused into isolated sections of the wafer.

To create the first layer's circuitry, a liquid photoresist is applied and baked onto the wafer. A mask plate is positioned into a jig and a wafer is placed beneath the mask plate and aligned with it. Ultraviolet light passes through the transparent regions of the mask plate and hardens the exposed photoresist. The wafer is then washed with an organic solvent to remove the non-exposed photoresist. What remains is a mask pattern laid out in hardened photoresist on the wafer's surface. The oxide layer that is not covered by photoresist is next removed by an acid solution. The surviving hardened photoresist is subsequently removed with a chemical bath. This process allows dopants to be diffused into the silicon where the openings in the oxide layer have been selectively made.

A dopant that will appropriately regulate the electrical conductivity of the silicon is selected and deposited across the whole surface of the wafer; the wafer is then again washed with acid to remove the dopant-blocking oxide.

Next, the wafer is placed inside an oxygen-ported oven and a silicon dioxide layer is grown over the areas covered by dopant. The wafer is then removed from the oven and placed inside a furnace where the dopant is driven into the silicon by controlled diffusion. This process of oxide growth, deposition, and diffusion is repeated in a series of up to dozens of masking steps. The chips become multiple layers of pure silicon, silicon dioxide, polycrystalline silicon and dopants. Again, it is subtle differences of dopant type and concentration between neighboring regions that impart circuit characteristics to the regions.

The circuits are interconnected by a metallization layer of an aluminum alloy containing silicon and copper. The alloy is vaporized in a vacuum chamber and deposited across the wafer. At the conclusion of the fabrication process a thin coating of oxide is placed over the wafer to form a protective or "passivation" coating. Each individual chip or "die" is then electrically tested for its ability to perform the operations for which it was designed. Any die that fails the test is marked with an ink blot and later discarded. Data generated from the electrical test is analyzed to improve the yield of future chip batches. The wafers are scribed and cut into individual dies, handled with vacuum tipped wands, and packaged. For an excellent discussion of semiconductor fabrication, see PLETSCH, *supra* note 75, at 45.

119. Stephen J. Davidson, *Reverse Engineering and the Development of Compatible and Competitive Products Under United States Law*, 5 SANTA CLARA COMPUTER & HIGH TECH. L.J. 399, 401 (1989).

120. *Id.*

121. Kewanee v. Bicron, 416 U.S. 470, 476 (1974).

122. *See, e.g.*, Brooktree Corp. v. Advanced Micro Devices, Inc., 705 F. Supp. 491, 495 (S.D. Cal. 1988).

123. "Again, you would measure the first layer on your computer; you etch it away, and now you have the second layer exposed. You measure that very carefully and etch it away. You continue to do that until . . . you have the set of complete patterns." *S. 1201 Hearings*, *supra* note 31, at 65 (statement of F. Thomas Dunlap, Jr., General Counsel, Intel Corp.).

124. Small rectangular areas on the corner of the chip which served no function at all were apparently copied. *H.R. 1007 Hearings*, *supra* note 30, at 26-27 (statement of L.J. Sevin, President, Mostek Corp.)

125. A similar copying incident involving Intel and NEC was reported four years later. Dan Morgan, *Battling to Innovate and Emulate: Intel Versus Nippon Electric*, WASH. POST, May 2, 1983, at A1 [hereinafter *Intel Versus Nippon Electric*].

126. The chip's design may not have been published because it was state-of-the-art at the time.

127. *See H.R. 1007 Hearings*, *supra* note 30, at 34-37 (composite photographs of piracy examples).

128. Scaling down the size of MOS transistors by a constant *K* reduces the propagation delay between transistors by 1/*K* and reduces power consumption by 1/*K*2. FREDERIKSEN, *supra* note 84, at 60.

129. "[A] reverse engineering firm could then improve the performance of the chip, reduce the size of the chip . . . . Here we have a true cost reduction or advancement in the state of the art." *H.R. 1028 Hearings*, *supra* note 34, at 28 (statement of F. Thomas Dunlap, General Counsel, Intel Corp.).

130. For example, in a DMOS process (not used in the 4K SRAM) the basewidth of transistors is narrowed by making use of differences in diffusion depths. FREDERIKSEN, *supra* note 84, at 59.

131. The preceding comparison was made during a June 1986 conversation with the general manager of a major Silicon Valley company. It should be noted that the comparison was made on the basis of composite photographs and, therefore, is limited.

132. *H.R. 1028 Hearings*, *supra* note 34, at 32 (statement of F. Thomas Dunlap, General Counsel, Intel Corp.).

133. *H.R. 1007 Hearings*, *supra* note 30, at 40 (statement of Andrew S. Grove, President, Intel Corp.).

134. Another notorious example of slavish copying also involved a pre-1979 design. The Intel 8086 microprocessor was first introduced in 1978. In 1980 NEC produced its own version of the 8086, a slavish copy that went so far in mimicing the original as to copy two tiny transistors disconnected and dangling from the chip in a useless bed of silicon. The two unneeded transistors were the result of a small last-minute repair job performed by Intel. *See Intel Versus Nippon Electric*, *supra* note 125, at A1.

135. *H.R. 1007 Hearings*, *supra* note 30, at 40 (statement of Andrew S. Grove, President, Intel Corp.).

136. *Id*. at 26-27 (statement of L.J. Sevin, President, Mostek Corp.).

137. *S. 1201 Hearings*, *supra* note 31, at 65 (statement of F. Thomas Dunlap, General Counsel, Intel Corp.).

138. *Id.* at 84.

> 139. [W]hen one attempts to copy mask sets, the problem is not quite as simple as merely copying a set of masks and putting the copied product into production using those masks. Rather, one has to have a process compatible with the design rules used in a mask and, so, our perception of the problem may be that the natural burdens in trying to adapt a similar process to use such a mask is in itself a barrier to the problem.

H.R. 1007 Hearings, *supra* note 30, at 64 (statement of Alan McPherson, Counsel, Fairchild Camera & Instrument Corp.).

"[I]t is not a simple matter of taking a chip or copy of a design and just running that in production. This would imply that processes are exactly the same from company to company. All of us in this business know that is not true." *Id.* at 69-70 (statement of John Finch, National Semiconductor).

140. "[C]ircuit designs are so intricate and complicated . . . that any attempt to make geometrical changes in the layout just for the sake of change will meet with disaster." *Id.* at 27 (statement of L.J. Sevin, President, Mostek Corp.).

141. The differing process obstacle to slavish copying is eventually solved, but not before a significant amount of time has passed.

> So really, obviously, the proprietary information is protected from the point of view that we don't let our process information out, but . . . most of the companies in the industry have very similar kind of processes, not exactly the same, but after a chip has been out for a year or two, maybe 6 months even, the processes have caught up to the point where the chip pirates can reproduce the same chip.

Id. at 42 (statement of Roger Borovoy, General Counsel, Intel Corp.).

142. The history of semiconductors has been one of continuous miniaturization. Medium scale integration (MSI) was achieved in 1970 when 2,000 transistors and 10-micron line widths were standard. Twenty thousand transistors and 6-micron line widths were prevalent by 1975 and this came to be known as large scale integration (LSI). Chips bearing as many as 200,000 transistors and line width densities of 4 microns were common in the 1980's, and are referred to by the acronym VLSI (very large scale integration). SPINKS, *supra* note 79, at 2-3. Today's era, with sub-micron feature sizes and transistor integration exceeding 1 million, has been named Ultra Large Scale Integration (ULSI).

Note the following trend since the 1983 SCPA Congressional Hearing Testimony:

Wafer Diameter 4" 5" 6" 8"

Year 1983 1985 1987 1989-91

Device 64K DRAM 256K DRAM 1MB DRAM 4MB DRAM

Process Steps 132 170+ 300+ 450+

Mask Levels 7 10 15 20

Feature Size (μm) 2.5 1.5 1.0 0.8

Defect Tolerance 0.25 0.15 0.10 0.08

CVD/PVD Steps 7 10 15 15

Surface Contamination 18 24+ 35+ 45+

Removal Steps

Table provided courtesy of Advantage Technologies (on file with author).

143. As stated *supra* part IV.A.3, timing verification and test pattern generation ordinarily require that the original design first be reverse engineered to its circuit diagram. The diagram is then subject to timing verification analysis before test patterns can be generated, fault graded, and pared down to the appropriate sequence of patterns. Thus, although the necessity of testing would seem to imply that there is an inherently substantial reverse and forward engineering burden to "knocking off a chip," that burden is sometimes removed by specialized reverse engineering companies. These companies have historically practiced reverse engineering on commodity high volume RAM and microprocessor products. "Canned" test programs developed by these companies are commercially available. *See How 'Silicon Spies' Get Away with Copying*, BUS. WK., Aug. 21, 1980, at 187.

144. Today's most advanced chips have circuit features of 0.8 microns and greater than a million transistors. *See* Don Clark, *US May Bounce Back in Key Chip Industry,* S.F. CHRON., May 21, 1991, at C1.

145. *See supra* note 143.

146. *Hearings on S. 646 and H.R. 6927 Before Subcomm. No. 3 of the House Comm. on the Judiciary*, 92d Cong., 1st Sess. (1971) [hereinafter *S. 646 and H.R. 6927 Hearings*].

147. *See Copyright Law Revision: Hearings on H.R. 2223 Before the Subcomm. on Courts, Civil Liberties and the Admin. of Justice of the House Comm. on the Judiciary,* 94th Cong., 1st Sess. (1976) [hereinafter *H.R. 2223 Hearings*].

148. "What has changed since 1965 is . . . the seriousness of the [piracy] problem, which is linked to the growing use of tape cartridges and cassettes. The ease of duplicating methods, their low cost, and the lack of clear statutory sanctions, have encouraged the so-called pirates." *S. 646 and H.R. 6927 Hearings, supra* note 146, at 11 (statement of Barbara A. Ringer, Assistant Register of Copyrights).

> With the development of consumer acceptance of tape, and the development of high speed tape duplicators, the need for protection became greater because it was easier to become a pirate; you bought a tape machine and set up operation in your garage. . . . [S]imilarly, when typeface design became embodied in photographic form, to become a pirate all you needed was a camera, and you copied the photo.

H.R. 1007 Hearings, supra note 30, at 11 (testimony of Jon Baumgarten, General Counsel, U.S. Copyright Office, Library of Congress).

149. Typeface designs can be easily copied by computerized photographic processes. *See H.R. 2223 Hearings, supra* note 147, at 1018-19 (statement of Joseph Gastel, attorney, International Typeface Corp.).

Typeface designs were subsequently held not to be copyrightable. Eltra Corp. v. Ringer, 579 F.2d 294 (4th Cir. 1978).

150. *See supra* part V.B.

151. *See supra* notes 139-41.

152. *H.R. 1028 Hearings, supra* note 34, at 375-79.

153. "Moral companies enter into cross-licensing agreements as if their designs were copyrightable." *H.R. 1007 Hearings, supra* note 30, at 42 (statement of Andrew Grove, President, Intel Corp.).

154. *See supra* note 57.

155. H.R. 14,293 is discussed *supra* note 38 and accompanying text; H.R. 1007 is discussed *supra* note 40 and accompanying text.

156. S. 1201, 98th Cong., 1st Sess. (1984), *discussed supra* text accompanying note 54.

157. H.R. 5525 REP., *supra* note 15, at 22.

158. *See* Kastenmeier & Remington, *supra* note 26, at 418-20.

159. *See supra* note 1.

160. Brooktree Corp. v. Advanced Micro Devices, Inc., 977 F.2d 1555, 1563 (Fed. Cir. 1992).

161. The two mask works were allegedly pirated from chips labeled Bt451 and Bt458. The mask works involved the location and configuration of the active areas in the static RAM (SRAM) cells and the location and path of the polysilicon lines in the SRAM cells.

Brooktree maintained that the mask works contained a great deal of originality: their design provided several important benefits including allowing one of the chips to (1) utilize the high frequency, low power CMOS fabrication technology without needing a special negative voltage supply; (2) change the colors in the color palette for display on a video screen without disrupting the selection of particular colors from the palette; and (3) operate at very high frequencies while simultaneously reading information from, and writing information to, the RAM without synchronizing the read and write operations. Brooktree Corp. v. Advanced Micro Devices, Inc., 707 F. Supp. 491, 494 (S.D. Cal. 1988).

162. *Id.* at 495-96.

163. *Id*.

164. *Brooktree*, 707 F. Supp. at 496.

165. Arguably, that a substantial dispute existed as to the true facts of the case furnished a strong reason to deny temporary relief. *See* DAN B. DOBBS, HANDBOOK ON THE LAW OF REMEDIES § 2.10, at 109 (1973).

166. *Brooktree*, 707 F. Supp. at 496-97.

167. *Id*. at 497 (emphasis added).

168. The degree of harm necessary to grant relief after a full scale trial is not necessarily enough to support temporary relief. *See* DOBBS, *supra* note 164, at 108-09.

169. *See supra* note 1; Brooktree Corp. v. Advanced Micro Devices, Inc., 757 F. Supp. 1088 (S.D. Cal. 1990).

170. Brooktree Corp. v. Advanced Micro Devices, Inc., 977 F.2d 1555 (Fed. Cir. 1992).

171. *Id.* at 1564. In the district court, AMD had moved for a new trial based on erroneous jury instructions. The jury was instructed:

> To establish infringement, Brooktree must show that A.M.D.'s mask works are substantially similar to a material portion of the mask works in Brooktree's chips covered by Brooktree's mask work registration. No hard and fast rule or percentage governs what constitutes a, quote, "substantial similarity." Substantial similarity may exist where an important part of the mask work is copied, even though the percentage of the entire chip which is copied may be relatively small. It is not required the A.M.D. make a copy of the entire mask work embodied in the Brooktree chip.

Id. AMD stated that the disputed instructions wrongly permitted the jury to impose liability by comparing only a portion of the AMD chip for substantial similarity, rather than comparing the entire mask work as a whole. The district court denied the motion, holding that recovery under the Act required only that "AMD misappropriated a material portion of the mask work." *Brooktree*, 757 F. Supp. at 1095 (citing Brooktree Corp. v. Advanced Micro Devices, 705 F. Supp. 491, 494 (S.D. Cal. 1988)).

172. *Brooktree*, 977 F.2d at 1564. In the district court, AMD had filed a motion for judgment notwithstanding the verdict claiming that in view of its "substantial investment in developing [the] second source product (along with an accompanying paper trail)," "no reasonable jury could have found that AMD did not prove its reverse engineering defense." 757 F. Supp. at 1092-93. The district court held that since "at least two of the elements of the [reverse engineering] defense-whether the AMD analysis of Brooktree's mask work was of the type contemplated by the Chip Act and whether the mask works were 'original'-were strongly contested" with credible evidence by Brooktree, AMD had failed to make out a case. *Id.*

173. *Brooktree*, 977 F.2d at 1569.

174. *Id.*; *see* 17 U.S.C. § 906(a) (1988).

175. *Brooktree*, 977 F.2d at 1570.

176. *Id.* at 1567. The jury was instructed:

> Reverse engineering is permitted and is authorized by the Chip Protection Act. It is not infringement of an owner's exclusive right and protected mask work for another person, through reverse-engineering, to photograph and to study the mask work for the purpose of analyzing its . . . circuitry, logic flow and organization of the components used in the mask work and to incorporate such analysis into an original mask work.
>
> The end product of the reverse-engineering process may be an original mask work, and therefore not an infringing mask work, if the resulting semiconductor chip product is not substantially identical to the protected mask work and its design involved significant toil and investment so that it is not mere plagiarism.
>
> You should place great weight on the existence of [a] reverse paperwork trail in determining whether the defendant's mask work is an original mask from reverse-engineering.
>
> A.M.D. mask work constitutes an original mask work if A.M.D.'s mask work incorporates its own new design elements which offered improvements over or an alternative to Brooktree's mask work.

Id.

177. *Id.* at 1570. Much of AMD's paper trail of time and expense was apparently spent pursuing dead ends. *Id.* at 1569.

178. *See supra* notes 142-45 and accompanying text.

179. However, if the prediction of one chip protection proponent is correct, it is the certainty of protection that dried up 90% of all piracy activity. *See H.R. 1007 Hearings*, *supra* note 30, at 44 (statement of Andrew S. Grove, President, Intel Corp.).

180. *See* Clark, *supra* note 109, at B1.

181. *See Creating Chips an Atom at a Time*, BUS. WK., July 29, 1991, at 54, 54-55.